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L3	446	716/14	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:05
L4	5	(716/13).ccls. and (ASIC same route) and (buffer or repeater)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:11
L5	6	(716/12).ccls. and (ASIC same route) and (buffer or repeater)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:07
L6	2	(716/14).ccls. and (ASIC same route) and (buffer or repeater)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:07
L7	63	("716"/\$.ccls. and (ASIC same route) and (buffer or repeater)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:07
L8	264	(ASIC same route) and (buffer or repeater)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:07
L9	9	(ASIC same route) and (buffer or repeater) and (transmission adj line)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:10
L10	1	(ASIC same route) same (buffer or repeater) same (transmission adj line)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:13
L11	3	(716/13).ccls. and ((ASIC same route) same (buffer or repeater))	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:12
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L13	0	(716/14).ccls. and ((ASIC same route) same (buffer or repeater))	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:13
L14	0	(716/14).ccls. and ((ASIC same route) same (buffer or repeater))	EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/25 12:13
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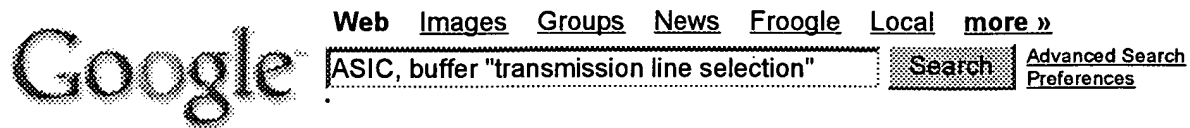
IEEE CNF IEE Conference Proceeding

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- ☐ 1. **An adaptive CMOS transmission line driver**
Patel, H.N.; Hohl, J.H.; Oalusinski, O.A.;
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27 Sept.-1 Oct. 1993 Page(s):460 - 463
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- ☐ 2. **Optimum repeater insertion based on a CMOS delay model for on-chip RLC inter**
Ismail, Y.I.; Friedman, E.G.;
ASIC Conference 1998. Proceedings. Eleventh Annual IEEE International
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- ☐ 3. **Embedded at-speed test probe**
Aigner, M.;
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1-6 Nov. 1997 Page(s):932 - 937
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- ☐ 4. **Package clock distribution design optimization for high-speed and low-power VL**
Qing Zhu; Tam, S.;
Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging
Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE
Volume 20, Issue 1, Feb. 1997 Page(s):56 - 63
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